Specification Amendments

Please replace paragraph [0048] with the following rewritten paragraph:

[0048] In the semiconductor fabrication industry, silicon oxide (SiO_2) is frequently used for its insulating properties as a gate oxide or dielectric. As the dimensions of device circuits on substrates become increasingly smaller, the gate dielectric thickness must decrease proportionately in field effect transistors (FETs) to approximately 3 to 3.5 n[[o]]anometers. Accordingly, device performance and reliability can be adversely affected by such factors as interfacial defects, defect precursors and diffusion of dopants through gate dielectrics, as well as unintended variations in thickness in the gate oxide layer among central and peripheral regions of the layer.

Please replace paragraph [0070] with the following rewritten paragraph:

[0070] The substrate [[10]] 32 is typically a silicon semiconductor wafer and may include active and passive IC devices fabricated within the wafer. Additionally or alternatively, devices may be fabricated in layers formed on the wafer. The substrate [[10]] 32 may be a semiconductor wafer of any size; for

example, an eight- or twelve-inch diameter wafer. The gate oxide layer 34 is preferably silicon dioxide and has a thickness of typically about 10~100 angstroms.

Please replace paragraph [0072] with the following rewritten paragraph:

[0072] The polysilicon layer 36 (referred to herein as polysilicon) may be either pre-doped polysilicon or amorphous silicon. After deposition of the polysilicon layer 36 on the gate oxide layer 34, the ~~the~~ polysilicon layer 36 may be annealed to cause diffusion of dopant ions throughout the polysilicon layer 36. The polysilicon anneal step also activates the chemical bonds between the dopant atoms and the silicon atoms in the polysilicon, such that the dopant atoms become a part of the crystalline polysilicon lattice structure in a process known as electrical activation. Alternatively, the polysilicon anneal step may be omitted.

Please replace paragraph [0074] with the following rewritten paragraph:

[0074] The resist layer [[22]] 42 is formed over the BARC layer 40 and patterned, exposed and developed to form the pattern that defines the polysilicon gate and other device structures to be fabricated on the substrate [[12]] 32. The resist layer

[[22]] 42 is preferably a DUV positive photoresist such as IBM APEX resist, IBM KRS resist, Hoechst Ax's DX-46, OCG's ARCH resists, Shinetsu, Tok, AZ or JSR. The resist layer [[22]] 42 can be any photoresist material such as a negative photoresist, and preferably has a thickness of typically about 1000~10000 angstroms and a width of typically about 0.05~0.30 μm.

Please replace paragraph [0077] with the following rewritten paragraph:

[0077] As shown in Figure 2D and process step S4 of Figure 3, the resist layer 42 and the underlying BARC layer 40 are stripped from the polysilicon layer 36. Accordingly, the patterned and etched hard mask layer 38 remains on the upper surface of the polysilicon layer 36. The resist and BARC stripping process is carried out in an HDP chamber, typically a TCP reactor with separate source and bias control. A biased O_2 plasma is used to strip the BARC layer 40 from the hard mask layer 38. A small quantity of C_2F_6 may be added to the process to enhance stripping of the BARC layer 40, as deemed necessary. Typical process parameters for the stripping process are as follows: chamber pressure (5~80 mTorr, preferably, 20 mtorr); TCP power (100~1500W ~~mTorr~~, preferably, 300W ~~mtorr~~); bias power (100~1500W ~~Ttorr, preferably, 0 mTorr~~); O_2 flow rate (50~500 sccm, preferably, 200 sccm).

U.S.S.N. 10,804,449

Please replace paragraph [0079] with the following rewritten paragraph:

[0079] Referring next to Figure 2E and step S5 of Figure 3, in the partial-etch step, a fluorine-based gas is used to partially etch the polysilicon layer 36 according to the pattern defined by the patterned and etched hard mask layer 38. The fluorine-based etching process is typically carried out in a high density plasma (HDP) etch chamber. The fluorine-based etchant gas may include a source gas such as fluorocarbon, fluoronitride a fluorine and nitrogen containing gas, or ~~fluorosulfur~~ a fluorine and sulfur containing gas, in non-exclusive particular. Application of the fluorine-based etchant gas in the partial etch step is typically followed by the complete etch step, which utilizes an etchant gas devoid of fluorine and typically having chlorine, bromine, oxygen and helium to enhance etching profile uniformity in the sidewalls of the etched polysilicon layer 36.

Please replace paragraph [0080] with the following rewritten paragraph:

[0080] Typical process parameters for the fluorine-based partial-etch step S5 include a chamber pressure of typically from about 5 mTorr to typically about 80 mTorr; a source radio frequency power of from typically about 100 watts to about 1500 watts at a source radio frequency of 13.56 MHz; a bias power of

from typically about 50 to typically about 1500 watts; and a fluorine-based etchant gas flow rate of typically about 100 sccm.

Please replace paragraph [0083] with the following rewritten paragraph:

[0083] Typical process parameters for the non-fluorine-based complete-etch step S6 include a chamber pressure of typically about 5~30 mTorr, and preferably, about 10 mTorr; a source radio frequency power of typically about 100~1500 watts, and preferably, about 150 watts, at a source radio frequency of 13.56 MHz; a bias power of typically about 100~1500 watts, and preferably, about 150 watts; a Cl_2 gas flow rate of typically about 20~500 sccm, and preferably, about 50 sccm; a He gas flow rate and an O_2 gas flow rate of typically about 10~500 sccm, and preferably, about 15 sccm; and an HBr gas flow rate of typically about 10~500 sccm, and preferably, about 150 sccm.